BINARY ADDER
&
BINARY SUBTRACTOR

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Objectives:

- 1. Half Adder.
- 2. Full Adder.
- 3. Binary Adder.
- 4. Binary Subtractor.
- 5. Binary Adder-Subtractor.

1. Half Adder

Half Adder: is a combinational circuit that performs the addition of two bit, this circuit needs two binary inputs and two binary outputs.

Inputs		Outputs	
X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Truth table

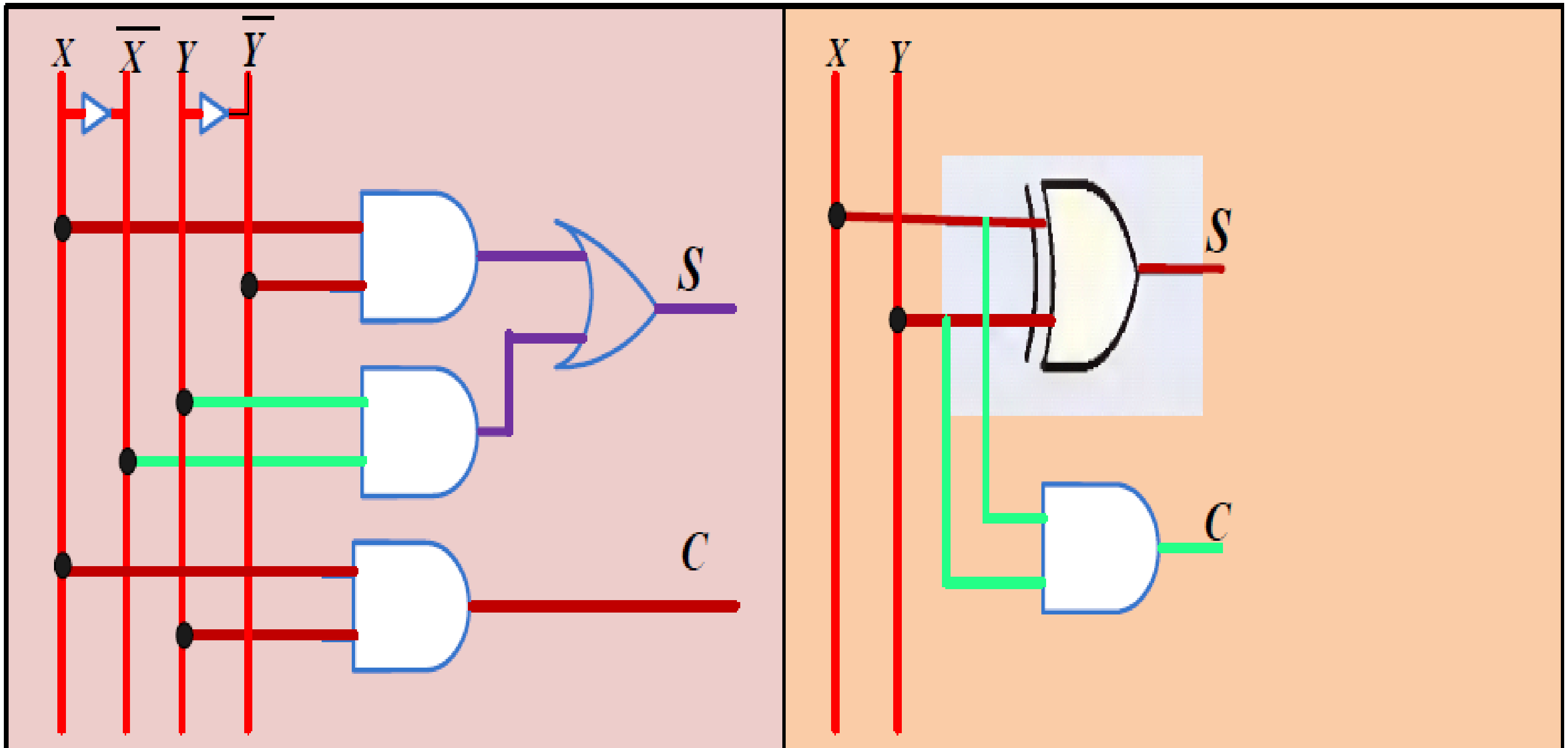
The simplified Boolean function from the truth table:

$$\begin{cases} S = \bar{X}Y + X\bar{Y} \\ C = XY \end{cases} \quad 1 \text{ (Using sum of product form)}$$

Where ***S*** is the sum and ***C*** is the carry.

$$\begin{cases} S = X \oplus Y \\ C = XY \end{cases} \quad 2 \text{ (Using XOR and AND Gates)}$$

- The implementation of half adder using ***exclusive–OR*** and an ***AND*** gates is used to show that two half adders can be used to construct a full adder.
- The inputs to the ***XOR*** gate are also the inputs to the ***AND*** gate.



Implementation of Half Adder using equation (1)

Implementation of Half Adder using equation (2)

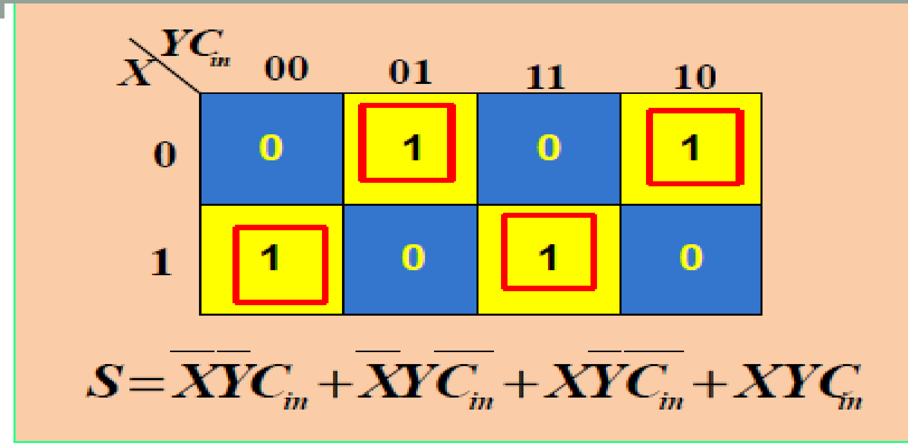
2. Full Adder

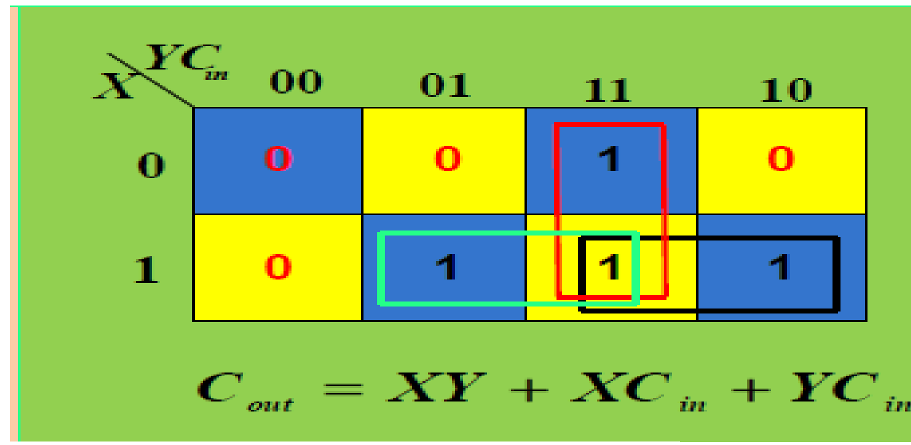
Full Adder :is a combinational circuit that performs the addition of three bits (two significant bits and previous carry).

- It consists of ***three inputs and two outputs***, two inputs are the bits to be added, the third input represents the carry form the previous position.
- The full adder is usually a component in a cascade of adders, which add 8, 16, etc, binary numbers.

Inputs			Outputs	
X	*Y*	C_{in}	*S*	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

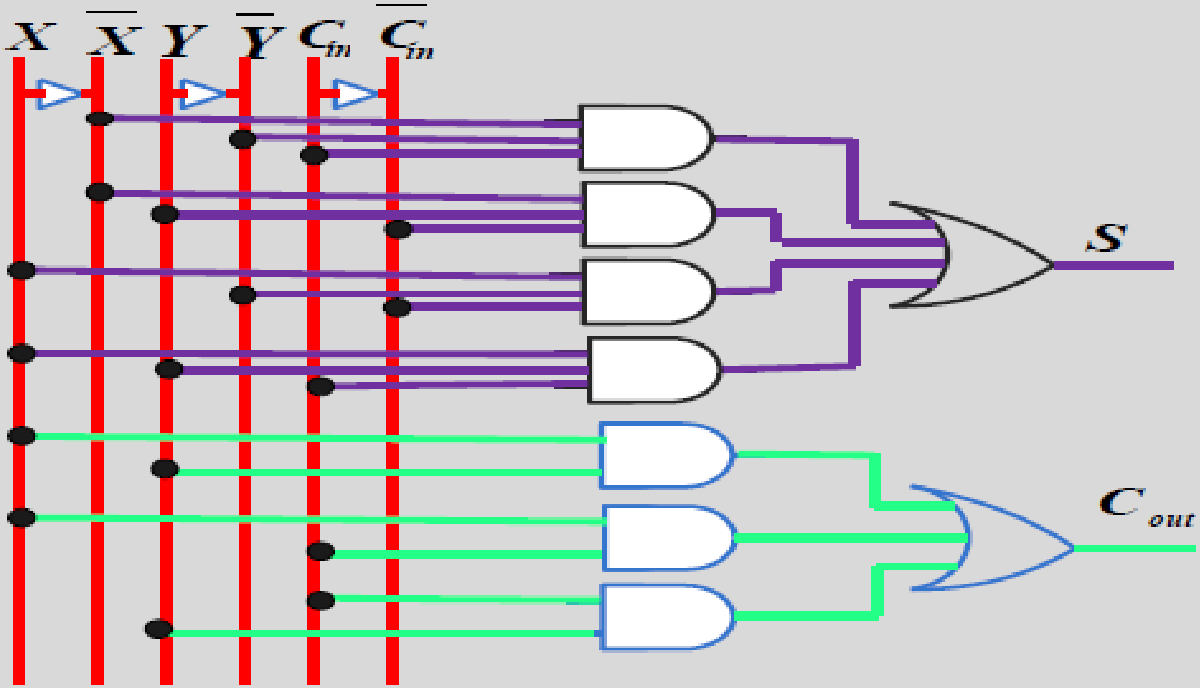
Truth table for the full adder





$$\left.\begin{aligned} S &= \bar{X}\bar{Y}C_{in} + \bar{X}Y\overline{C_{in}} + X\bar{Y}\overline{C_{in}} + XYC_{in} \\ C_{out} &= XY + XC_{in} + YC_{in} \end{aligned}\right\} \quad 1 \ \textit{(Sum of products)}$$

- The *logic diagrams* for the full adder implemented in *sum-of-products* form are the following:



logic diagram for the full adder

- It can also be implemented using ***two half adders*** and ***one OR gate*** (using **XOR** gates).

$$\begin{Bmatrix} S = C_{in} \oplus (X \oplus Y) \\ C_{out} = C_{in} \cdot (X \oplus Y) + XY \end{Bmatrix}$$

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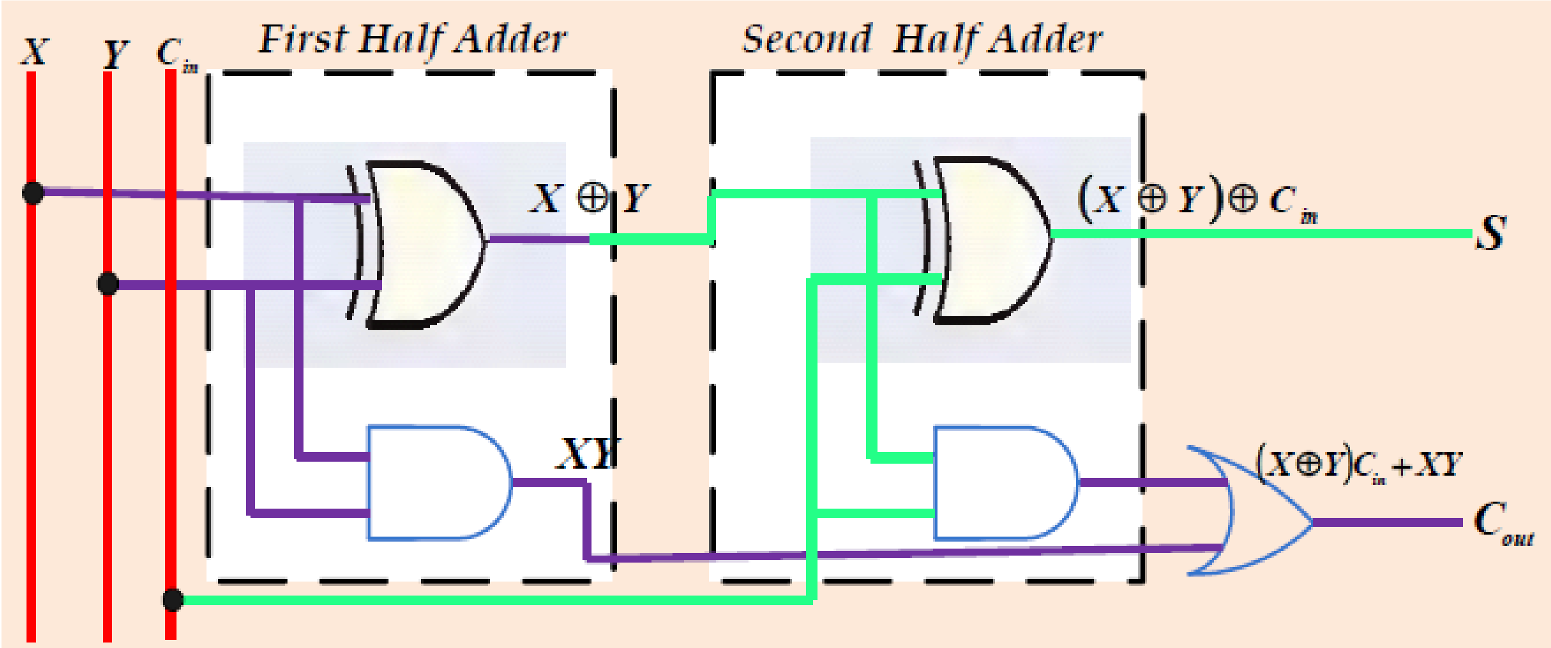
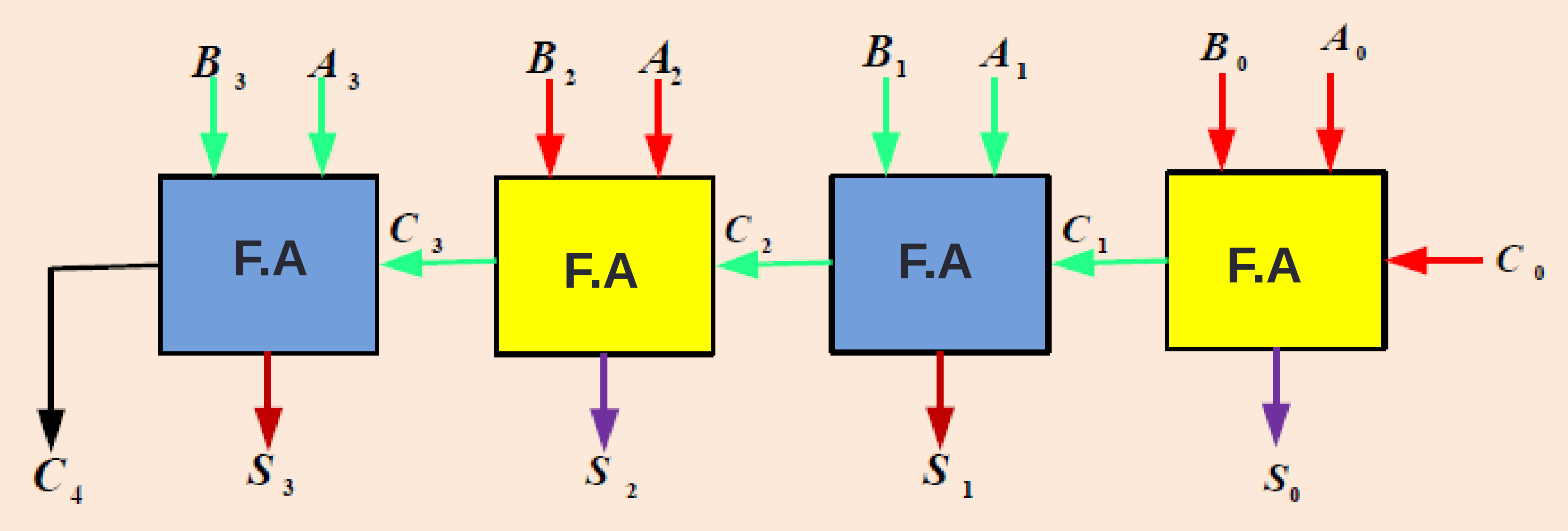


Implementation of Full Adder with two Half Adders and an OR gate

3. Binary Adder (Asynchronous Ripple-Carry Adder)

- A binary adder is a digital circuit that produces the ***arithmetic sum of two binary numbers***.
- A binary adder can be constructed with ***full adders connected in cascade*** with the output carry form each full adder connected to the input carry of the next full adder in the chain.
- The ***four-bit adder*** is a typical example of a ***standard component*** .It can be used in many application involving arithmetic operations.

- The input carry to the adder is C_0 and it ripples through the full adders to the output carry C_4.
- n-bit binary adder requires n full adders.



Four-bit Adder (Ripple Carry Adder)

Example:

$A + B$ $(A = 1011)$ and $(B = 0011)$

Subscript i	3	2	1	0		
Input Carry	0	1	1	0	C_i	
A	1	0	1	1	A_i	$C_0 = 0$
+						
B	0	0	1	1	B_i	
Sum	1	1	1	0	S_i	
Output Carry	0	0	1	1	C_{i+1}	

H.W

- using (4-bit Ripple-Carry Adder) Implement the following:

  X+ 2Y (each one 3-bit)

  4X+Y (x 2-bit , y 3-bit)

- Given a =111 , b =101 , c = 1100

  Implement a+b+c using full Adder blocks.

4. Binary Subtractor ：

- To perform the subtraction $-B$, we can use the ***2's complements***, so the subtraction can be converted to addition.

- ***2's complement*** can be obtained by talking the ***1's complement*** and adding ***1*** to the ***LSD*** bit.

  1) ***1's complement*** can be implemented with inventors.

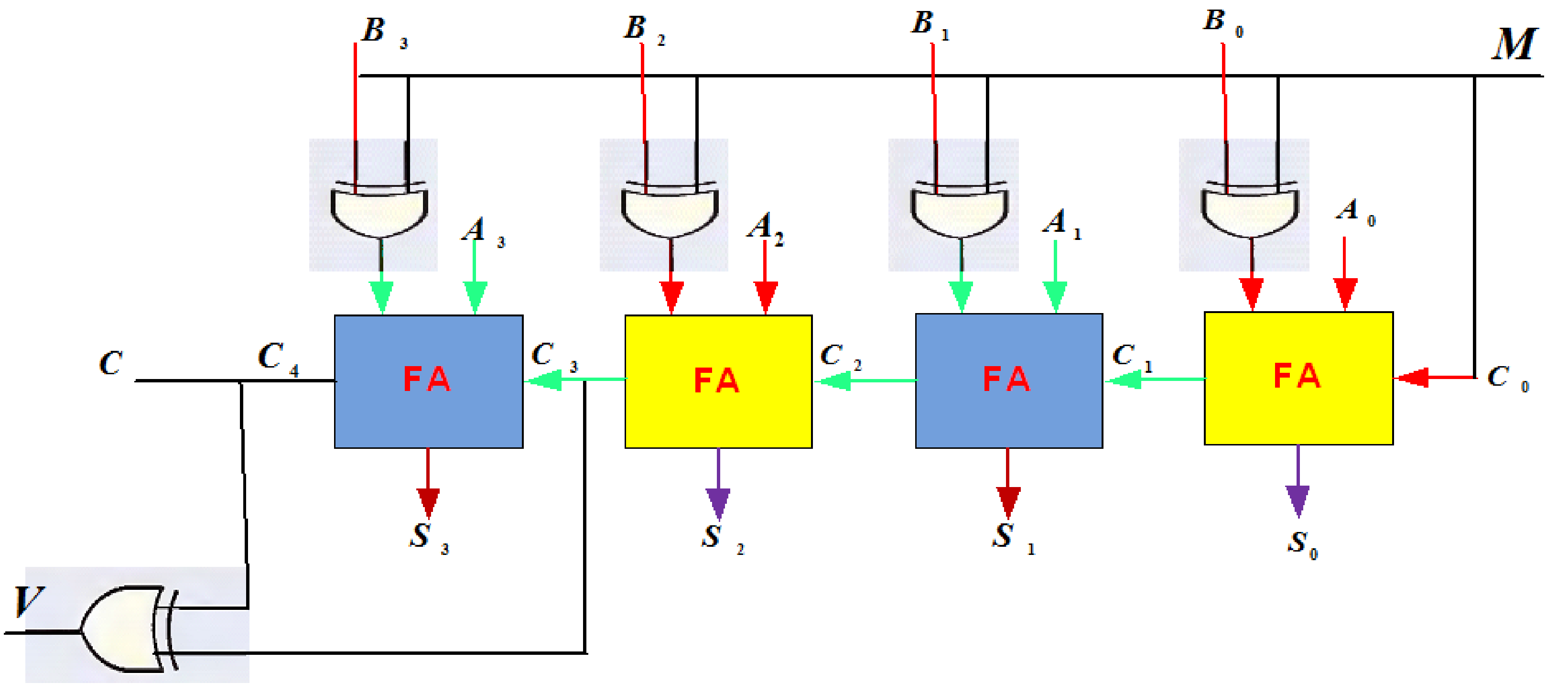
  2) ***1*** can be added to the sum through the input carry.

- The circuit for subtracting $A-B$ consists of an adder with inverters placed between each data input B and the corresponding input of the full adder.

  The input carry C_0 must be equal to 1.

5. Binary Adder–Subtractor

- The addition and subtraction operations can be combined into one circuit with one common binary adder by including an *exclusive-OR* gate with each full-adder.



Four-bit Binary Adder–Subtractor

The mode input M controls the operation as the following:

- o $M = 0 \rightarrow$ adder.
- o $M = 1 \rightarrow$ subtractor.

- Each XOR gate receives M signal and B
  - o When $M = 0$ then $B \oplus 0 = B$ and the carry = **0,** then the circuit performs the operation $A + B$.
  - o When $M = 1$ then $B \oplus 1 = \overline{B}$ and the carry = **1,** then the circuit performs the operation $A - B$.

- The *exclusive-OR* with output V is for detecting an overflow.

H.W

- using (4-bit Binary Adder–Subtractor)Implement the following:

  X+ 2Y (each one 3-bit)

  4X-Y (x 2-bit , y 3-bit)

- using (4-bit Binary Adder–Subtractor) Find:
  - 9 - 5
  - 15 - 6

Thank You